AN3424
Application note

STEVAL-ILL042V1: high power factor flyback LED driver based on the L6562A and TSM101

Introduction

The high-PF flyback configuration, used to drive a new design of the 60 W LED array, is based on the L6562A and the TSM101 controller (*Figure 1*).

This configuration uses an isolated feedback with an optocoupler and a secondary side reference/error amplifier, the TSM101, for voltage and current regulation.
The TSM101 includes two op amps: one op amp is used for constant voltage control and the other for constant current control. A precise internal current generator, available, can be used to offset the intervention threshold of the constant current regulation.

The L6562A is a PFC controller operating in transition-mode. The highly linear multiplier includes a special circuit, able to reduce AC input current distortion, that allows wide-range-mains operation with an extremely low THD, even over a large load range.

The TSM101 compares the DC voltage and current level of a switching power supply to an internal reference. It provides a feedback through an optocoupler to the L6562A controller in the primary side.

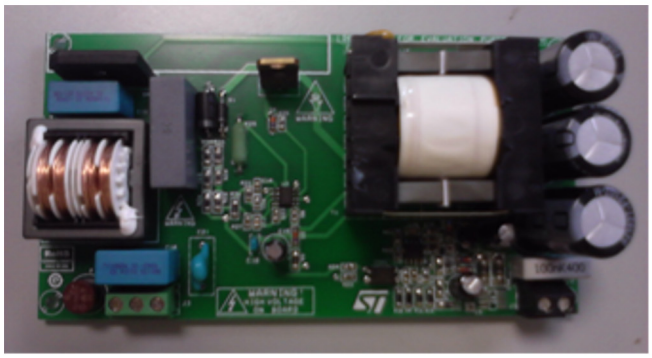
This system, designed by using the L6562A and the TSM101 controller, offers more advantages in terms of output current and voltage stability.

The input capacitance is so small here that the input voltage is very close to a rectified sinewave. Besides, the control loop has a narrow bandwidth so as to be little sensitive to the twice-mains frequency ripple appearing at the output.

Efficiency is high at heavy load, more than 90% is achievable: TM operation ensures slow turn-on losses in the MOSFET and the high PF reduces dissipation in the bridge rectifier.

The output voltage exhibits a considerable twice-mains frequency ripple, unavoidable if a high PF is desired. Speeding up the control loop may lead to a compromise between a reasonably low output ripple and a reasonably high PF. To keep the ripple low, a large output capacitance (in the thousand F) is anyway required.

Figure 1. Board image



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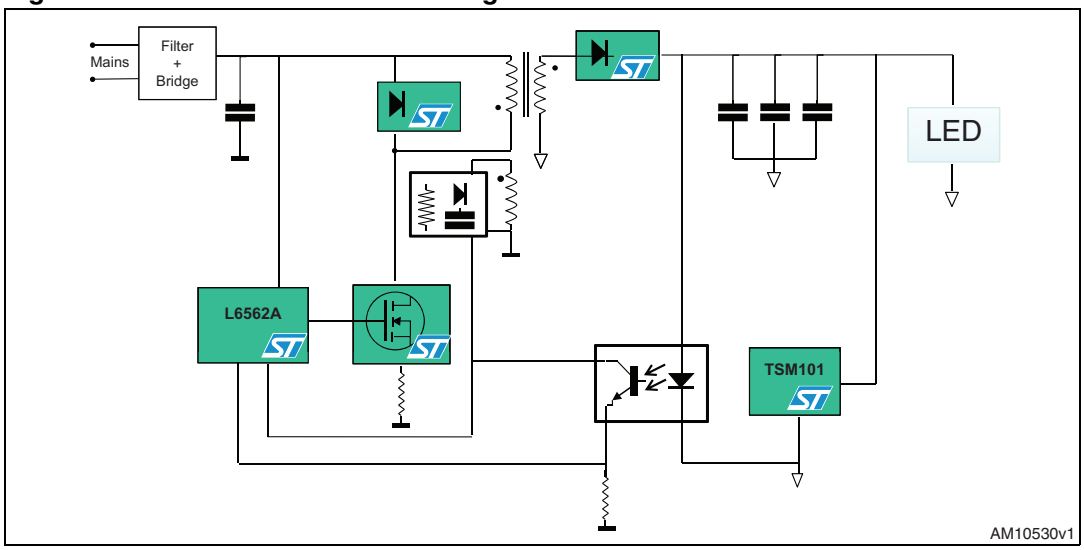
1 Board block diagram

Figure 2 shows a block diagram of the system. The complete circuit is made up of two stages:

- The flyback converter which regulates the output voltage and performs the power factor correction.
- The current and voltage controller stage which regulates the current and voltage output feedback.

This topology, thanks to STMicroelectronics ICs L6265A and TSM101, realizes a high-PF flyback converter with voltage and current output regulation.

Figure 2. 60 W LED driver block diagram



2 Electrical schematic and bill of material

Figure 3. Electrical schematic

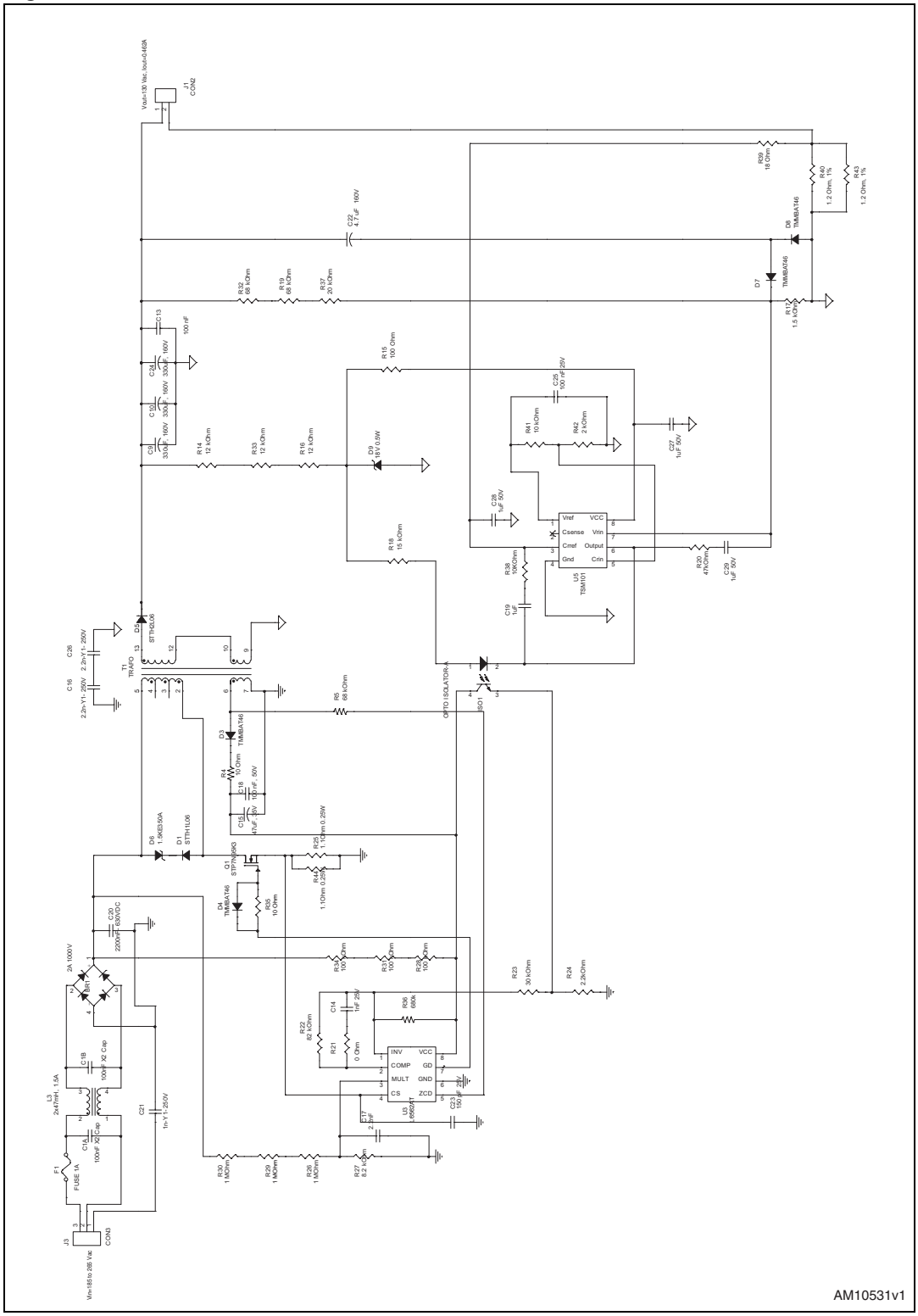


Table 1. Bill of material

Reference	Value	Rated	Type	Manufacturer
BR1		2 A/1000 V		
C1A, C1B	100 nF	275 Vac	Polypropylene film capacitor X2	
C9, C10, C24	330 µF	160 Vdc	Electrolytic capacitor	
C13	100 nF	250 Vdc	Polyester capacitor	
C14	1 nF	25 Vdc	COG ceramic capacitor	
C15	47 µF	35 Vdc	Electrolytic capacitor	
C16, C26	2.2 nF	250 Vac	Y1 capacitor	
C17	2.2 nF		X7R ceramic capacitor	
C18	100 nF	50 Vdc	X7R ceramic capacitor	
C19, R38	220 nF, 100 kΩ			
C20	220 nF	630 Vdc	Polypropylene film capacitor	
C21	1 nF	250 Vac	Y1 capacitor	
C22	4.7 µF	160 Vdc	Electrolytic capacitor	
C23	150 pF	25 V	Capacitor	
C25	100 nF	25 Vdc	X7R ceramic capacitor	
C27, C29	1 µF	50 Vdc	Ceramic capacitor	
C28	10 nF	50 Vdc	X7R ceramic capacitor	
D1	STTH1R06	1 A/600 V	Ultrafast diode	STMicroelectronics
D3, D4	TMMBAT 46	100 V		STMicroelectronics
D5	STTH2L06	2 A/600 V	Ultrafast diode	STMicroelectronics
D6	1.5KE350A	350 V/1.5 kW	Transil	STMicroelectronics
D7, D8	TMMBAT 46	150 mA/100 V		STMicroelectronics
D9		18 V/0.5 W	Zener diode	
F1		1 A/250 V	Fuse	
ISO1	PC817		OPTO ISOLATOR-A	
J1	CON2			
J3	CON3			
L3	2 x 47 mH	1.1 A	Common mode choke	

Table 1. Bill of material (continued)

Reference	Value	Rated	Type	Manufacturer
Q1	STP7N95K3	950 V/1.1 Ω	SuperMESH™III	STMicroelectronics
R4, R35	10 Ω	0.25 W		
R5, R19, R32	68 kΩ	0.25 W, 1%		
R14, R16, R33	12 kΩ	0.25 W		
R15	100 Ω	0.25 W		
R17	1.5 kΩ	0.25 W		
R18	15 kΩ	0.25 W		
R20	47 kΩ	0.25 W		
R22	82 kΩ			
R23	30 kΩ			
R24	2.2 kΩ	1%		
R25, R44	1.1 Ω	0.25 W, 1%	Metal film resistor	
R26, R29, R30	1 MΩ	0.25 W, 1%		
R27	8.2 kΩ	0.25 W, 1%		
R28, R31, R34	100 kΩ	0.25 W		
R36	680 kΩ	0.25 W, 1%		
R37	20 kΩ	0.25 W		
R39	18 Ω	0.25 W		
R40, R43	1.2 Ω	0.25 W, 1%	Metal film resistor	
R41	10 kΩ	1%		
R42	2 kΩ	1%		
T1	TRAFO	0.9 mH		
U3	L6562A		TM, PFC controller	STMicroelectronics
U5	TSM101		Voltage and current controller	STMicroelectronics

3 Design and calculation parameters

Figure 4. High-PF flyback characteristic functions: F1(x) diagram

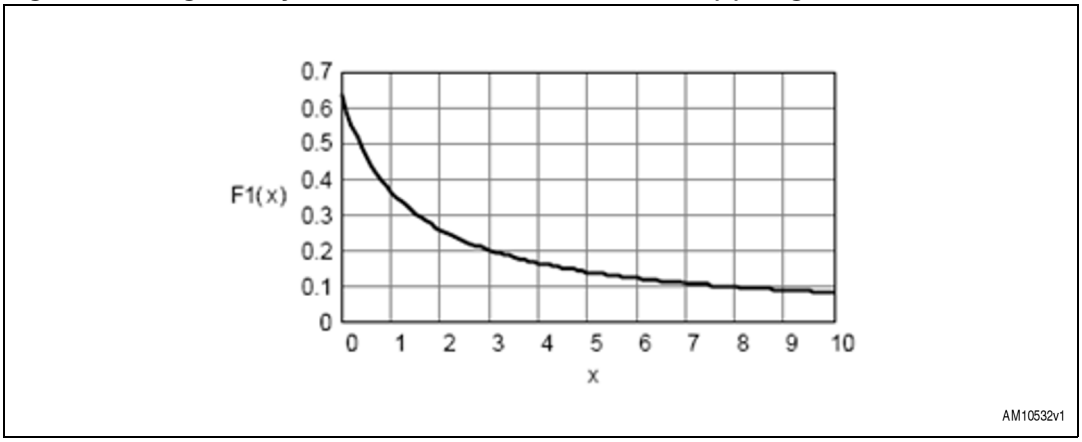
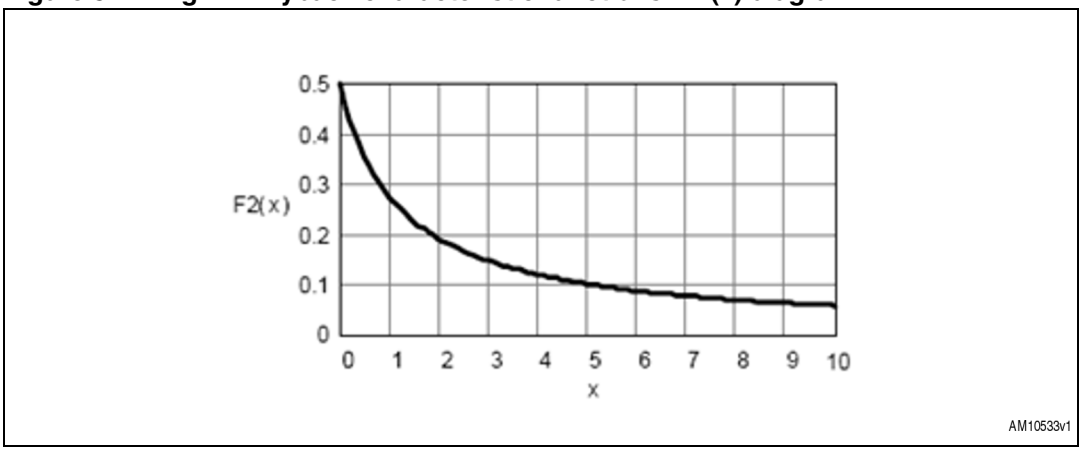


Figure 5. High-PF flyback characteristic functions: F2(x) diagram



The following is a step-by-step design of the L6562A-based high-PF flyback converter:

1. Design specifications:
   - Mains voltage range: V_{ACmin} = 185 Vac, V_{ACmax} = 265 Vac
   - Minimum mains frequency: f_L = 47 Hz
   - DC output voltage: V_{out} = 130 V
   - Maximum output current: Iout = 0.462 A
   - Maximum 2fL output ripple: $\Delta V_O\%$ = 1.0%
2. Pre-design choices:
   - Minimum switching frequency: f_{SWmin} = 57 Kz
   - Reflected voltage: V_R = 195 V
   - Leakage inductance spike: Vspike; 100 V
   - Expected efficiency: 92%
3. Preliminary calculations:
   - Minimum input peak voltage: $V_{PKmin} = V_{ACmin} \cdot \sqrt{2} = 185 \cdot \sqrt{2} - 4V = 257V$ (4 V total drop on $R_{DS(ON,\ RS,\ ...)}$

– Maximum input peak voltage: $V_{PKmin} = V_{ACmax} \cdot \sqrt{2} = 265 \cdot \sqrt{2} - 4V = 371V$

– Maximum output power: $P_{OUT} = V_{out} \cdot I_{out} = 130 \cdot 0.462 = 60W$

– Maximum input power: $P_{in} = \frac{P_{out}}{\eta} \cdot 100 = \frac{60}{92} \cdot 100 = 65.2W$

– Peak-to-reflected voltage ratio: $K_V = \frac{V_{PKmin}}{V_R} = \frac{257}{195} = 1.32$

– Characteristic functions value: F1(1.32) = 0.35, F2(1.32) = 0.24, F3(1.32) = 0.20

4. Operating conditions:

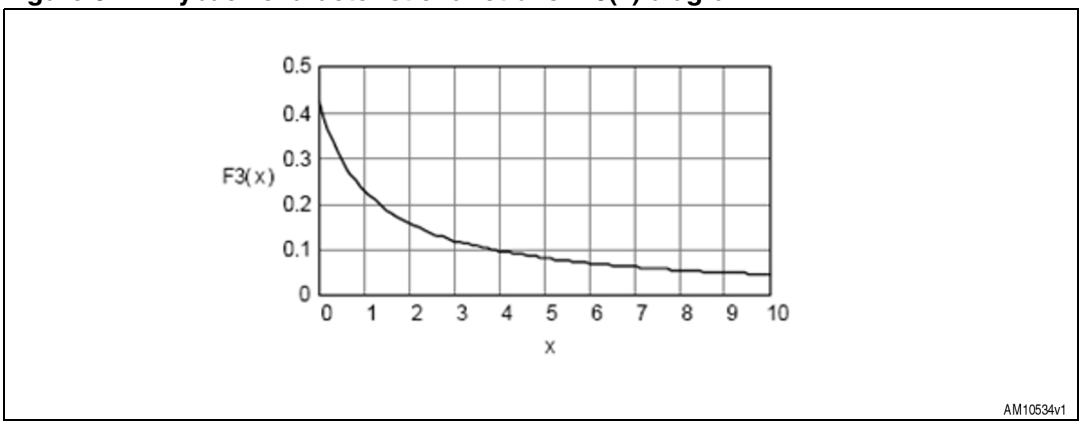
– Peak primary current: $I_{PKp} = \frac{2 \cdot P_{in}}{V_{PKmin} \cdot F2(K_V)} = \frac{2 \cdot 65.2}{257{,}6 \cdot 0.24} = 2.11A$

– RMS primary current: $I_{RMSp} = I_{PKp} \cdot \sqrt{\frac{F2(K_V)}{3}} = 2.11 \cdot \sqrt{\frac{0.24}{3}} = 0.595A$

– Peak secondary current: $I_{PKs} = \frac{2 \cdot I_{out}}{K_V \cdot F2(K_V)} = \frac{2 \cdot 0.462}{1.32 \cdot 0.24} = 2.916A$

– RMS secondary current: $I_{RMSs} = I_{PKs} \cdot \sqrt{K_V \cdot \frac{F3(K_V)}{3}} = 2.916 \cdot \sqrt{1.32 \cdot \frac{0.2}{3}} = 0.865A$

Figure 6. Flyback characteristic functions: F3(x) diagram



5. Primary inductance: $L_p = \frac{V_{PKmin}}{(1+K_V) \cdot f_{SWmin} \cdot I_{PKp}} = \frac{257.6}{(1+1.32) \cdot 57 \cdot 10^3 \cdot 2.11} = 0.922mH$

– Primary-to-secondary turns ratio: $n = \frac{V_R}{(V_{out} + V_f)} = \frac{195}{(130 + 0.6)} = 1.49$

– Minimum area product calculation:

$$A_{Pmin} = \left[\frac{460 \cdot P_{in}}{f_{SWmin} \cdot (1+K_V) \cdot \sqrt{F2(K_V)}} \right]^{1.316} = \left[\frac{460 \cdot 65.2}{57 \cdot 10^3 \cdot (1+1.32) \cdot \sqrt{0.24}} \right]^{1.316} = 0.363cm^4$$

This calculation highlights that the minimum AP required is about 0.36 cm^4. An ETD34 core (AP = 1.1175 cm^4) is used. This value of APmin reduces the number of turns N and simultaneously L_{lk} is reduced (leakage inductance) as reported in the following formulas:

Equation 1

$$AP_{min} = A_{min} \cdot A_N = A_e \cdot A_w = \frac{I_e \cdot L}{\mu_e \cdot \mu_o \cdot N^2} = \frac{L}{k \cdot N^2}$$

so, with primary and secondary inductance in the transformer fixed, the AP_{min} is inversely proportional to the square of the turns N.

This reduces strongly the power dissipation in the clamp network by increasing the system efficiency.

The ferrite used is N87, which guarantees low losses and high saturation.

Table 2. Gapped

Material	g (mm)	A_L value approx. nH	μ_e
N87	0.20 ± 0.02 0.50 ± 0.05 1.00 ± 0.05	482 251 153	310 161 98

In this specific design g = ≈1 mm, A_L is the inductance referred to number of turns = 1:

Equation 2

$$A_L = \frac{L}{N^2} = \frac{\mu_e \cdot \mu_o}{\frac{l_e}{A_e}}$$

where:

- μ_e, μ_0 are respectively effective permeability and magnetic field constant
- A_e is effective magnetic cross section

Table 3. Calculation factors

Material	Relationship between air gap - A_L value		Calculation of saturation current			
	K1 (25 °C)	K2 (25 °C)	K3 (25 °C)	K4 (25 °C)	K3 (25 °C)	K4 (25 °C)
N87	153	-0.713	240	-0.796	222	-0.873

Note: K1, K2:0.10 mm<s<2.50 mm.

K3, K4: 80 nH<A_L<780 nH.

6. MOSFET selection:

   Maximum drain voltage: $V_{DSmax} = V_{PKmax}+V_R+\Delta V = 372 + 195 + 100 = 667$ V

   There is some margin to select a 950 V device. This minimizes gate drive and capacitive losses. Assuming that the MOSFET dissipates 5% of the input power, that losses are due to conduction only, and that $R_{DS(on)}$ doubles at working temperature, the $R_{DS(on)}$ at 25 °C should be about 2 Ω. An STP7N95K3 ($R_{DS(on)}$ 1.35 Ω max.) in TO-220 Zener-protected SuperMESH3 is selected.

7. Catch diode selection:

   Maximum drain voltage: $V_{REV\,max} = \frac{V_{PK\,max}}{n} + V_{out} = \frac{371}{1.493} + 130 = 378V$.

   A suitable device is an STTH3L06, a TURBO 2 ultrafast high voltage rectifier with I_F = 3 A (minimum current rating is 1.166 A), V_{RRM} = 600 V ($V_{RRM}>V_{REVmax}$).

   From the relevant datasheet the power dissipation is estimated as:

Equation 3

$$P_{out} = V_f \cdot I_{out} + R_{th} \cdot I^2_{RMSs} = 0.89 \cdot 0.462 + 0.055 \cdot 0.86^2 = 0.45W$$

This means $T_j = T_{amb} + R_{th} \cdot P_{out} = 75 + 75 \cdot 0.45 = 108.75°C$, acceptable value.

8. Output capacitor selection:

   The minimum capacitance value that meets the specification on the 100/120 Hz ripple is:

Equation 4

$$C_{outmin} = \frac{1}{\pi \cdot f_L} \cdot \frac{H2(K_V)}{F2(K_V)} \cdot \frac{I_{out}}{\Delta V_o} = \frac{*0.462}{3.14 \cdot 47 \cdot 0.24 \cdot 1} = 1025\mu F$$

Three 330 µF electrolytic capacitors have an ESR low enough (max. 446 mΩ) to consider the high frequency ripple negligible as well as sufficient AC capability.

9. Clamp network:

   With a proper construction technique, the leakage inductance can be reduced less than 1% of the primary inductance, which it is in the present case. A Transil clamp is selected.

   The clamp voltage is $V_{CL} = V_R+\Delta V = 195 + 100 = 295$ V. The steady-state power dissipation is estimated to be about 1 W. A 1.5KE350A Transil is selected. The blocking diode is an STTH1L06.

10. Multiplier bias and sense resistor selection:

    Assuming a peak value of 2.6 (@ V_{AC} = 265 V) on the multiplier input (MULT, 3) the peak value at minimum line voltage is $V_{MULTpkmin} = 2.6 \cdot \frac{185}{265} = 1.81V$ which,

    multiplied by the maximum slope of the multiplier, 1, gives 1.81 V peak voltage on current sense (CS, pin 4).

    Since the linearity limit (3 V) is not exceeded, this is acceptable. The driver ratio is then $\frac{2.6}{(\sqrt{2} \cdot 265)} = 6.93 \cdot 10^{-3}$. Considering 260 µA for the divider, the lower resistor

is 10 kΩ, and the upper one 1 MΩ. Choose the sense resistor 0.5 Ω, while its power rating is $P_S = 0.5 \cdot I_{RMSp}^2 = 0.5 \cdot 0.595^2 = 177mW$.

11. Feedback and control loop:

The selected optocoupler is an ISO1-CNY-17.

The TSM101 is a voltage and current controller that regulates the output and current voltage provided to the LED.

By considering V_{out} = 130 V and that the value at pin 7 is compared to the internal 1.24 V band-gap voltage reference, the V_{pin7} is:

Equation 5

$$V_{pin7} = V_{out} \cdot \frac{R_6}{R_6 + R_7} = 130 \cdot \frac{1.5k}{1.5k + 156k} = 1.24V$$

with R_6 = 1.5 kΩ, R_7 = 156 kΩ.

R_5 = 0.6 Ω is the sense resistor used for current measurement. The current regulation is effective when the voltage drop across it is equal to the voltage on pin 5 of TSM101.

For medium currents (<1 A), a voltage drop across R_5 of 200 mV = V_{R5} is a good value, R_5 can be realized with standard low cost 0.4 W resistors in parallel.

Equation 6

$$R_5 = \frac{V_{R5}}{Ich} = 0.57\Omega \quad \text{(two 1.2 Ω resistors in parallel)}$$

R2 and R3 can be chosen using the following formula:

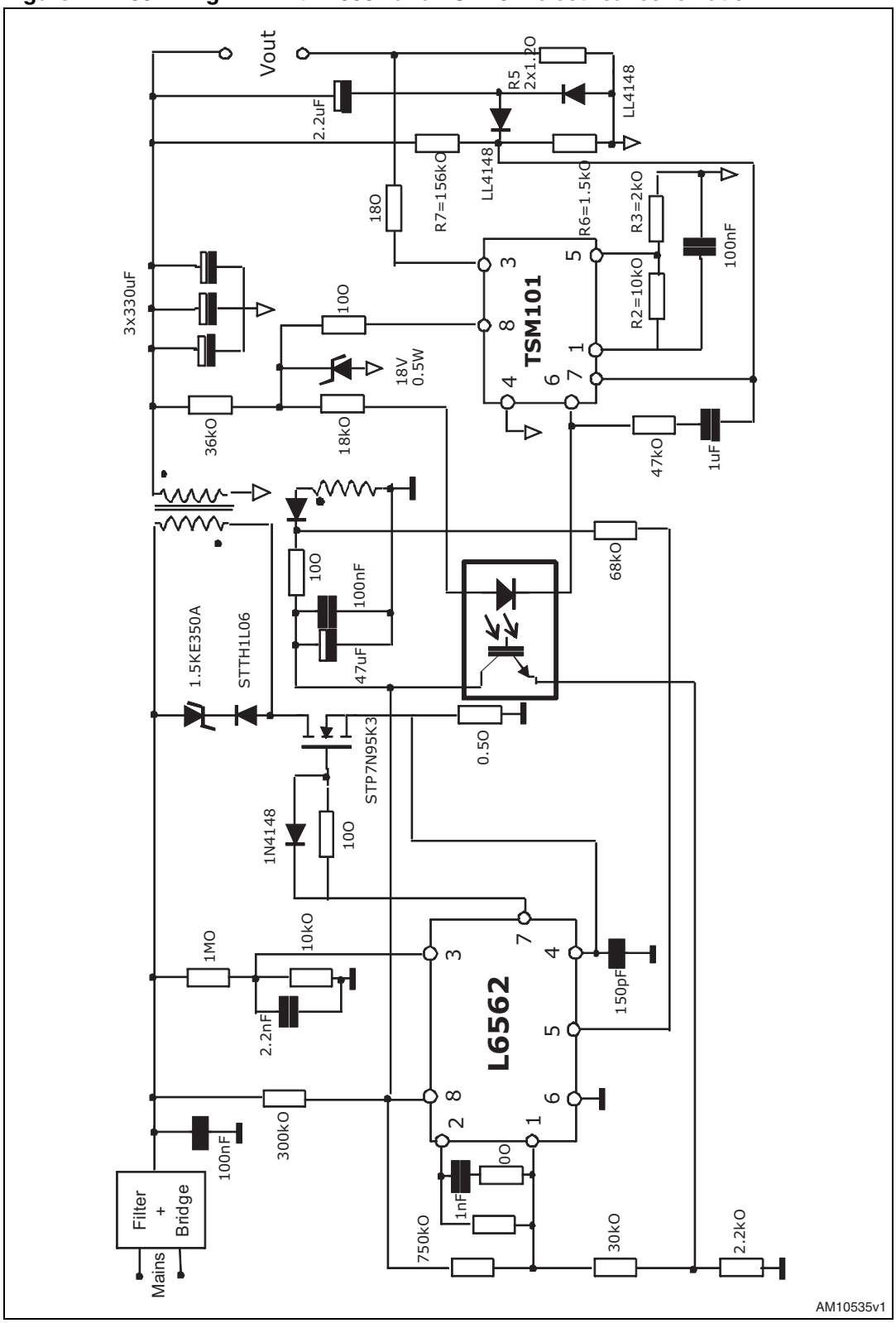
Equation 7

$$R_2 = R_3 \cdot \left(\frac{V_{ref} - V_{R5}}{V_{R5}} \right)$$

Fixed R_3 = 2 kΩ, we can have R_2 = 10 kΩ.

The complete electrical schematic of this application is illustrated in *Figure 7*.

Figure 7. 60 W high-PF with L6562 and TSM101: electrical schematic



12. Experimental results:
    These results have been obtained at input voltage between 185 and 265 V.
    Ambient temperature: 23 °C
    - V_{OUT} = 118.7 V
    - I_{OUT} = 358 mA
    - P_{OUT} = 42.5 W

Figure 8. Pin vs. Vin

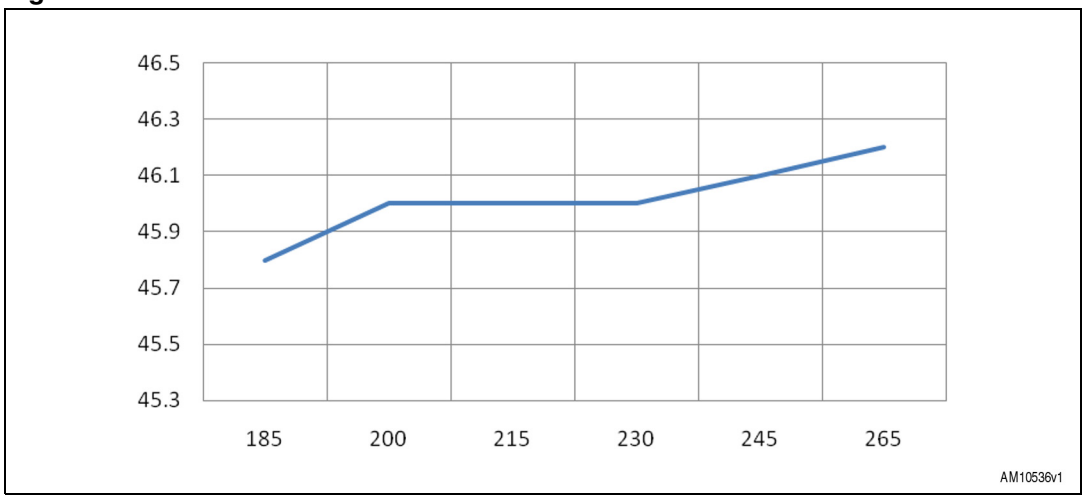


Figure 9. THD vs. Vin

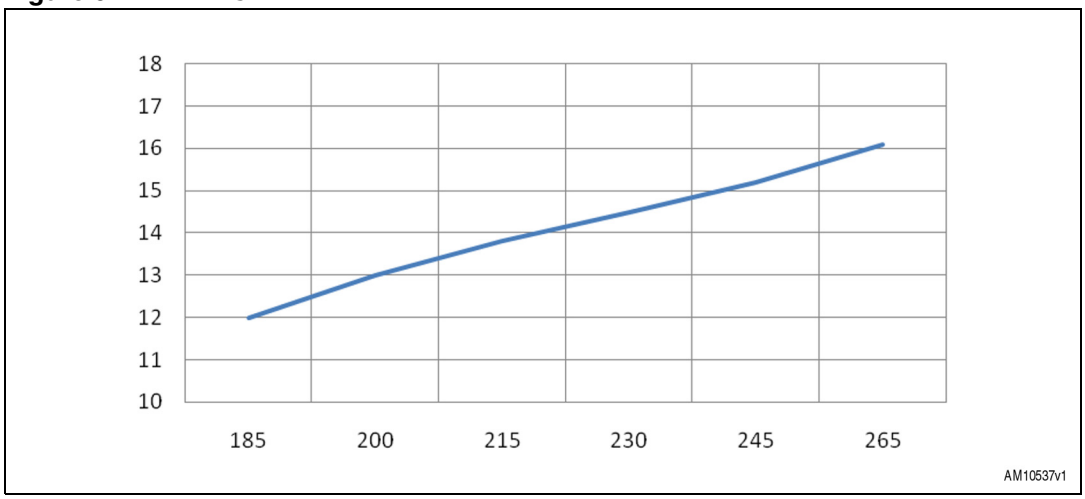


Figure 10. PF vs. Vin

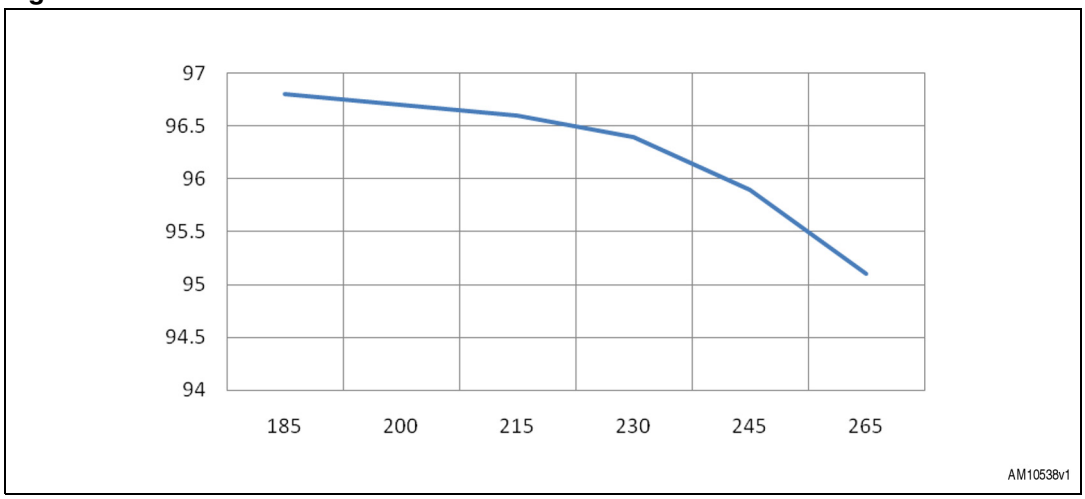


Figure 11. Efficiency vs. Vin

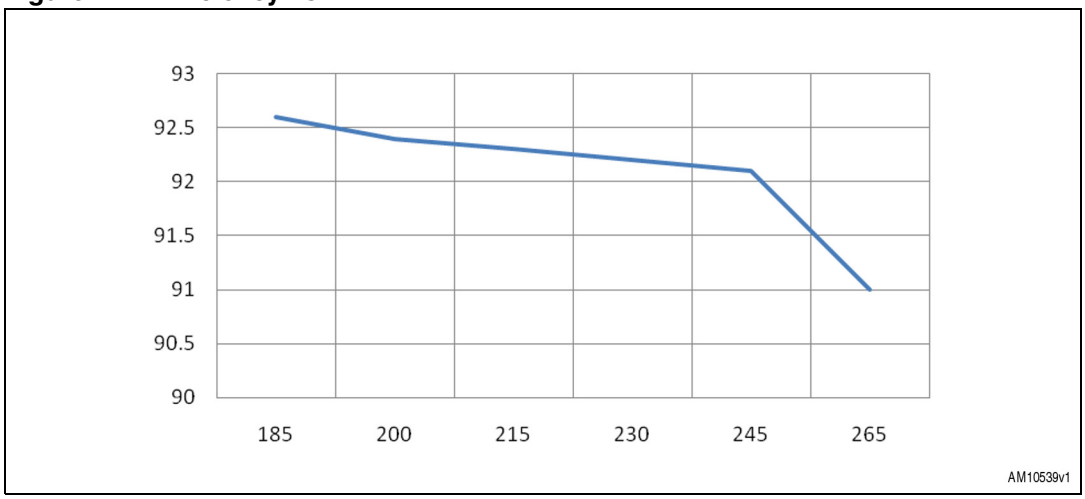


Figure 12. Startup @ 230 V L6562A Vcc (red) MOSFET drain voltage (brown)

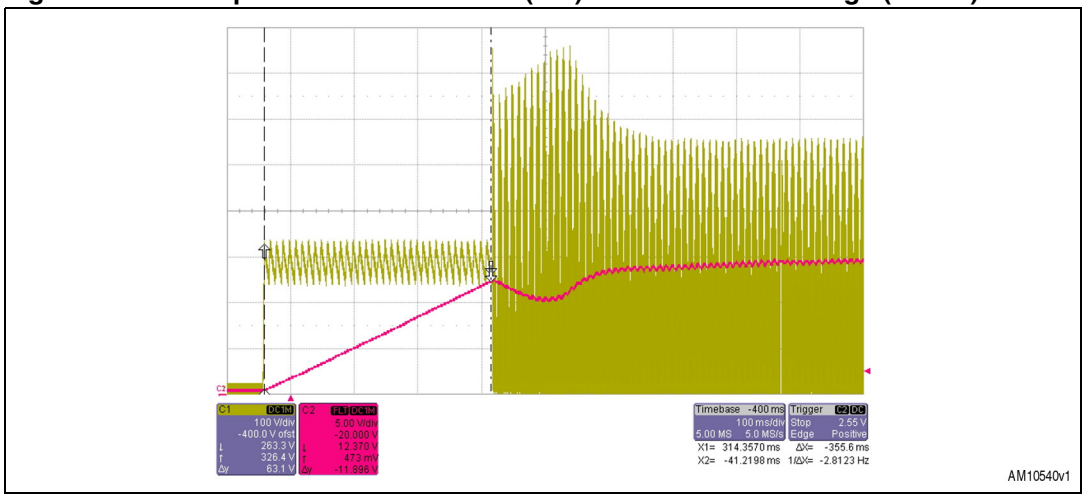


Figure 13. Startup 230 V - Iout (green), Vout (blue), L6562A Vcc (red)

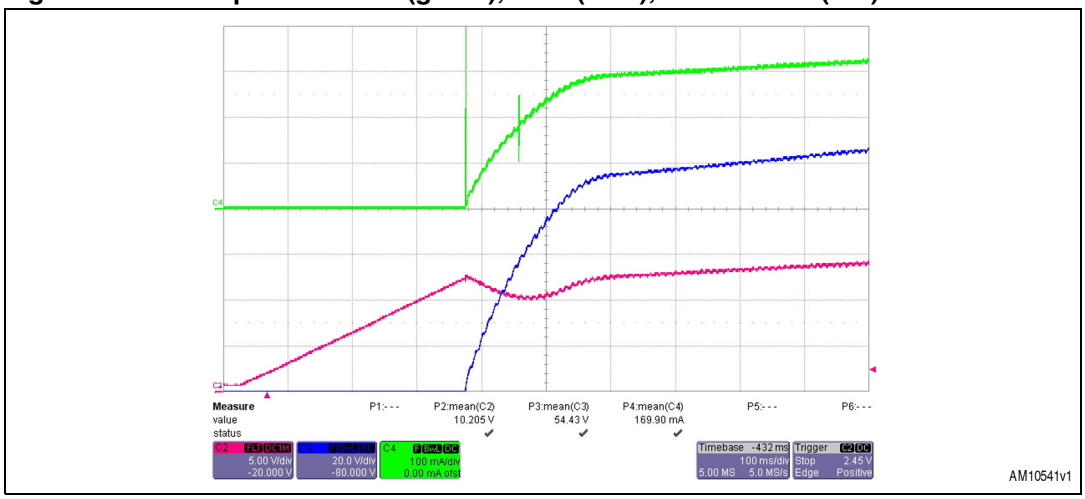


Figure 14. Vin, Iin. PFC @ 185 V

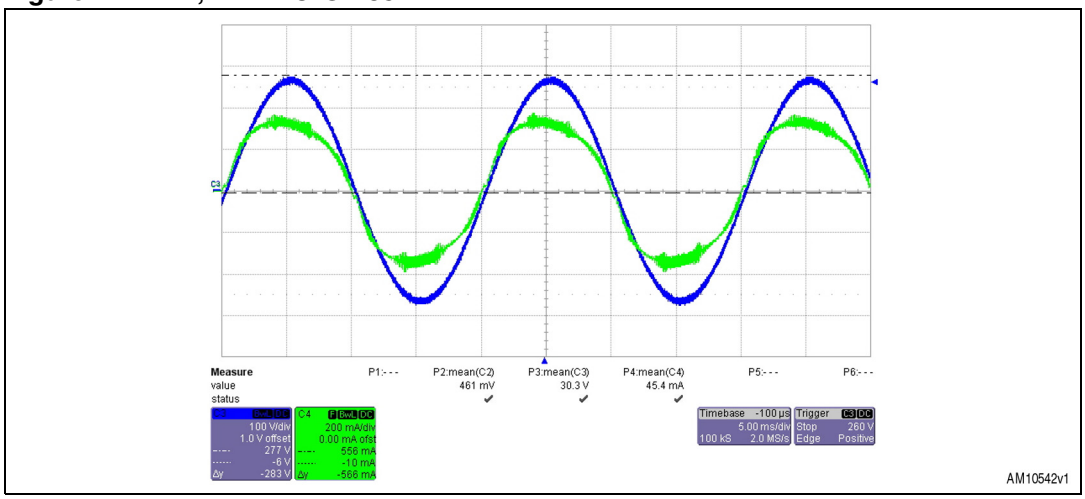


Figure 15. Vin, Iin. PFC @ 230

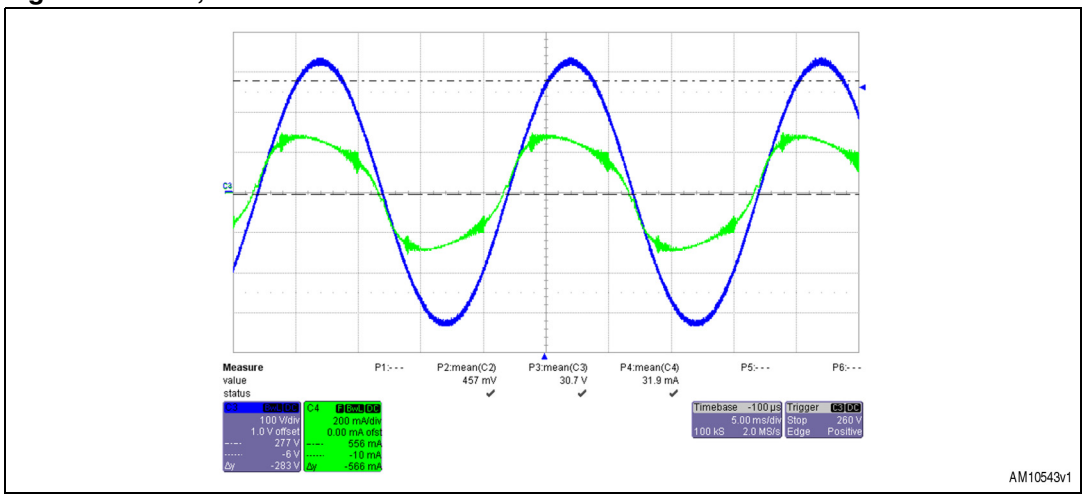
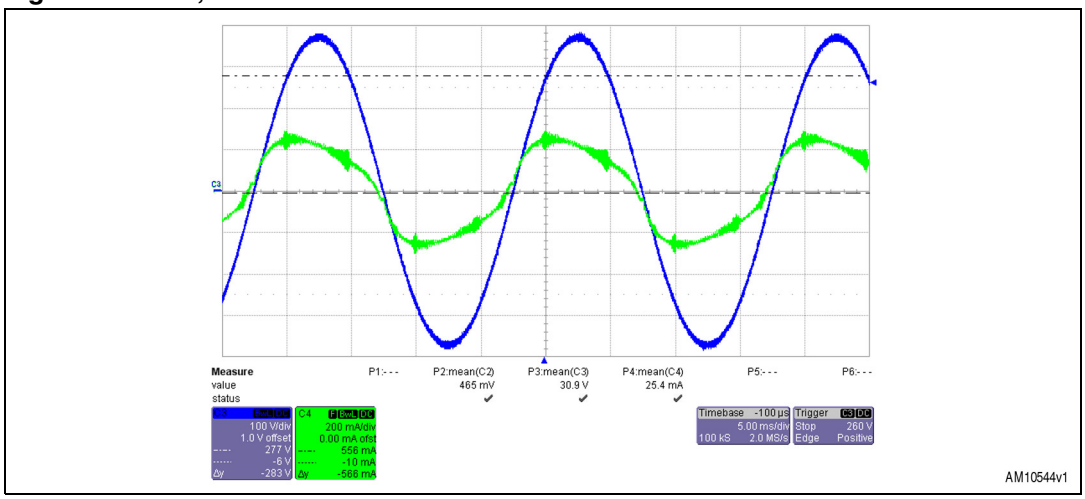


Figure 16. Vin, Iin. PFC @ 265 V



4 Thermal measurements

These measurements were performed at ambient temperature of 25 °C and at minimum input voltage (185 V, worst case for PFC section).

Thermal measurement on the power device was performed on the board using infrared thermocamera FLUKE.

For the PFC section, the temperature was measured on the power MOSFET and on the diode.

On the power MOSFET with a mounted heatsink, having thermal resistance R_{th} = 11.40 °C/W, the temperature on the top of the package was 40 °C. On the top of the Transil diode the temperature was 35 °C, for the clamp diode 35 °C, for the IC driver 47 °C, and for the output diode 55 °C.

5 EMC tests results

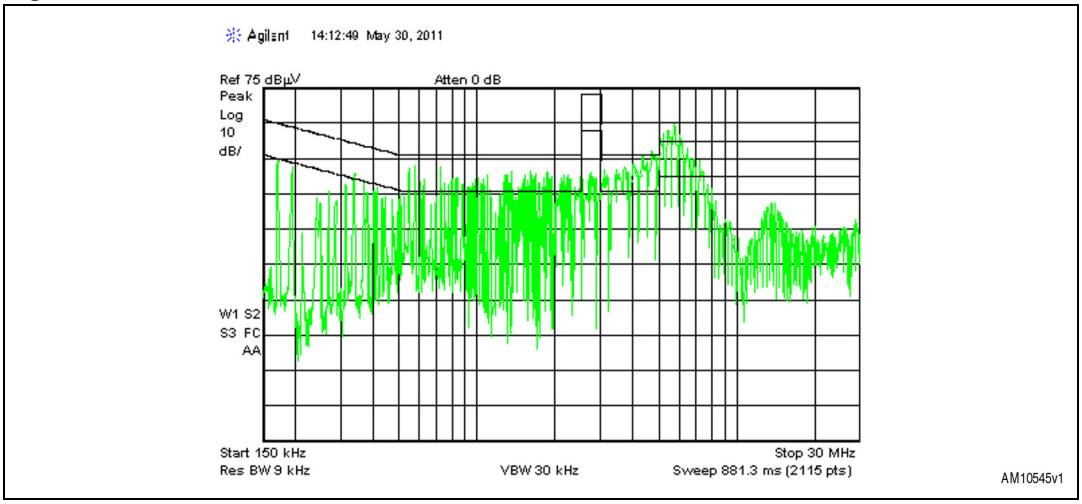
EMC test was conducted according to the EN55015A standard.

The test was performed using the following apparatus:

- EMC ANALYZER Agilent E7401A
- LISN EMCO model 3825/2, 50 Ω, 10 kHz - 100 MHz.

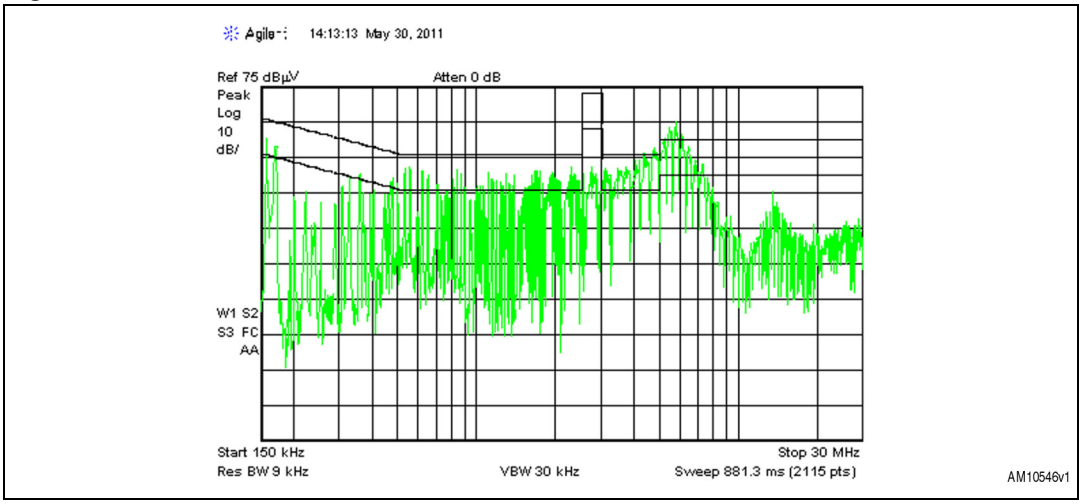
The test was performed using peak detector and the limits of average and quasi peak of EN 55015A standard in the range 150 kHz - 30 MHz at 230 V 50 Hz input voltage.

Figure 17. Peak measure: line wire



In *Figure 17* it is possible to observe that the conduced emissions are out of the limits in the range 5 - 6 MHz.

Figure 18. Peak measure: neutral wire



6 Conclusions

The high-PF flyback configuration used to drive a new design of the 60 W LED array and based on the PFC L6562A and on the voltage and current TSM101 controller works correctly in a single range [185 - 265] V. In the same range the efficiency is very high, more than 92% (*Figure 11*).

Thermal measurements show that the power MOSFET reaches T = 40 °C.

Thanks to the TSM101, the system offers an excellent LED current regulation in terms of current precision and works properly in all input conditions and output load, by offering high performance with a simple and reliable design.

7 Revision history

Table 4. Document revision history

Date	Revision	Changes
08-Nov-2011	1	Initial release.

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